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Microcomputer.

1. A microcomputer including a plurality of register banks in which different register banks can be accessible during the execution of one instruction is disclosed.

The microcomputer comprises a plurality of register banks each consisting of a plurality of registers for containing data therein, a bank address register for holding the address of one of said register banks to be accessed and access control means responsive to a bank address signal for putting one of said register banks in accessible condition.

The microcomputer is characterized by further comprising:

a logic gate circuit receiving at one input at least one bit of the address held in the bank address register and at another input a predetermined portion of the code of an instruction to be executed by the microcomputer and for modifying the inputted bit of the bank address; and

a selection circuit for selecting any one of the modified bit and the non-modified bit of the bank address and outputting the selected bit as at least a portion of the bank address signal to said access control means.

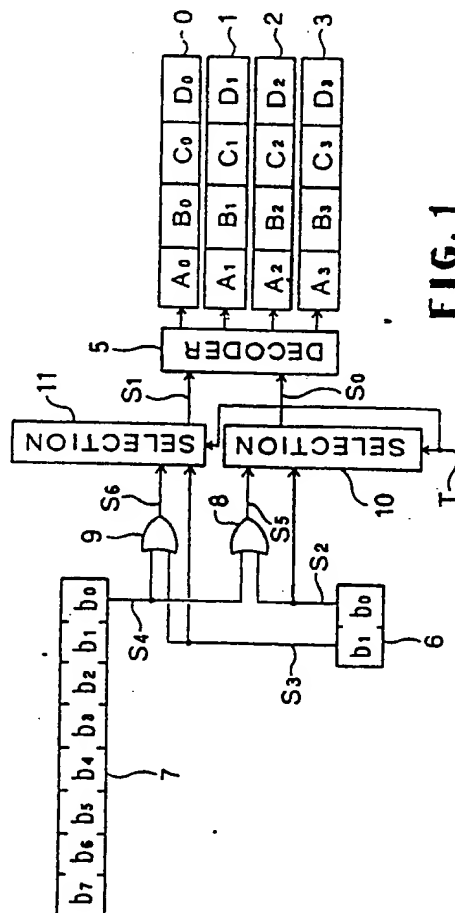


FIG. 1

## MICROCOMPUTER

## Background of the Invention

The present invention relates to a microcomputer including a plurality of register banks, of which any one bank is designated by means of a bank address register for processing data stored therein.

General purpose registers are widely employed for arithmetic calculation and comparing processing in the microcomputer, and thus the microcomputer must be equipped with a plurality of general purpose registers for storing therein the results of a variety of processings or data to be processed.

The microcomputer actually employed comprises a plurality of register banks, each consisting of a series of general purpose registers. Any one of the register banks is selected by means of a bank address register for each processing to be executed. In such a microcomputer, it is easy to execute a processing of data in a same register bank. For example, in case the contents in the registers A and B of the register bank 0 should be added with each other and the result should be stored in the register A of the register bank 0, the address of the register bank 0 is set to the bank address register and then an instruction for adding the content of the register A with that of the register B is executed. In case the content of the register A of the register bank 0 is to be added with that of the register B of the register bank 1 and that the result is to be stored in the register A of the register bank 0, however, the processing has to be executed by a plurality of instructions, because two different register banks cannot be accessed at the same time during the execution of one instruction. That is, in a first instruction, the bank register 1 is accessed by setting the address of the register bank 1 in the bank address register to transfer the content of the register B of the register bank 1 to a memory. With other instruction, the bank register 0 is accessed by setting the address of the register bank 1 in the bank address register to add the content of the register A of the register bank 1 with the content stored in the memory.

Such a complicated processing was conducted not only in the arithmetic processing but also in the transfer of data which should be often conducted. Namely, the processing of the data stored in different register banks has had to be accompanied with the transfer of data via memory.

Accordingly, the processing of the data stored in different register banks was complicated and required a program of which the steps were numerous. Thus, the execution time for such a processing was prolonged.

## Summary of the Invention

It is a main object of the present invention to provide a microcomputer which can execute data processing between different register banks at a high speed.

It is another object of the present invention to provide a microcomputer which can process data stored in different register banks by the execution of only one instruction.

According to the present invention, there is provided a microcomputer which includes a plurality of register banks each consisting of a plurality of registers for containing data therein, a bank address register for holding the address of one of said register banks to be accessed and access control means responsive to a bank address signal for putting one of said register banks in accessible condition, said microcomputer comprising:

a logic gate circuit receiving at one input at least one bit of the address held in the bank address register and at another input a predetermined portion of the code of an instruction to be executed by the microcomputer and for modifying the inputted bit of the bank address; and

a selection means for selecting any one of the modified bit and the non-modified bit of the bank address and outputting the selected bit as at least a portion of the bank address signal to said access control means.

According to an embodiment of the present invention, the logic gate circuit comprises, for example, an OR gate.

According to another embodiment of the present invention, the logic gate circuit comprises a first OR gate receiving at one input the least significant bit of the address (which is preferably coded in 2 bit length) held in the bank address register and at another input the least significant bit of the code of an instruction to be executed by the microcomputer and a second OR gate receiving at one input the most significant bit of the address held in the bank address register and at another input the least significant bit of the code of the instruction to be executed by the microcomputer.

According to a preferred embodiment of the present invention, the selection means comprises a first selection circuit receiving the output of the first OR gate and the least significant bit of the address held in the bank address register and for selecting any one thereof, and a second selection circuit receiving the output of the second OR gate and the most significant bit of the address held in the bank address register and for selecting any one thereof.

According to a still further preferred embodiment of the present invention, the first and second selection circuits are responsive to the variation of a timing signal to select one of the inputted signals.

According to a still further embodiment of the present invention, the logic gate circuit is constituted by an Exclusive OR gate receiving at one input the least significant bit of the address held in the bank address register and at another input the least significant bit of the code of an instruction to be executed by the microcomputer.

The other characteristics and advantages of the present invention will be understood clearly from the description of the examples which will be made with reference to the accompanying drawings in which:

## Brief Description of the Accompanying Drawings

Fig. 1 is a block diagram of the first example of the microcomputer embodying the present invention;

Fig. 2 is a block diagram of the second example of the microcomputer embodying the present invention; and

Fig. 3 is a block diagram of the third example of the microcomputer embodying the present invention.

## Description of the Preferred Embodiments

The microcomputer shown in Fig. 1 comprises registers arrayed in a matrix form of four rows and four columns.

Each row of the register matrix constitutes a register Bank 0 to 3. That is, the register bank 0 includes registers A., B., C, and D.. The register bank 1 includes registers A., B., C, and D.. The register bank 2 includes register A., B., C, and D., and the register bank 3 includes registers A., B., C, and D..

The microcomputer is equipped with a access control means of decoder 5. The decoder 5 receives bank designating signals S<sub>0</sub> and S<sub>1</sub>, and puts any one of the register banks 0 to 3 in accessible condition according to the combination of the bank designating signals S<sub>0</sub> and S<sub>1</sub>, as shown in Table 1.

Table 1

Bank designating signal		Register bank to be Designated
S <sub>0</sub>	S <sub>1</sub>	
0	0	0
0	1	1
1	0	2
1	1	3

The construction of the decoder 5 is well known in the art and thus it will not be explained here any more.

The microcomputer further comprises a bank address register 6 and an instruction register 7.

The bank address register 6 has two bit length in this example for storing the address of the register bank to be accessed. The bank address register 6 is set "00" for designating the register bank 0, "01" for the register bank 1, "10" for the register bank 2, and "11" for the register bank 3.

The instruction register 7 is a memory circuit for storing therein the code of a certain instruction to be executed by the microcomputer. In this example, the instruction register has eight bit length. In this example, the instruction code of the first transfer instruction for transferring the data contained in the register B to the register A in a same register bank is expressed as "10011000". On the other hand, the instruction code of the second transfer instruction for transferring the data from the register B to the register A in a same register bank or between different register banks is "10011001". Namely, the instruction code of the second transfer instruction is obtained by adding "1" to the least significant bit of the instruction code of the first transfer instruction.

The microcomputer comprises first and second OR gates 8 and 9. The first OR gate 8 receives signals S<sub>0</sub> and S<sub>1</sub>, which are respectively the contents b<sub>0</sub> stored in the least significant bit of the bank address register 6 and the instruction register 7. The first OR gate 8 outputs a logical sum signal S<sub>2</sub> of the signals S<sub>0</sub> and S<sub>1</sub>. The second OR gate 9 receives a signal S<sub>0</sub>, which is the content b<sub>1</sub> stored

in the most significant bit of the bank address register 6 and the signal S<sub>1</sub>, which is the content b<sub>2</sub> stored in the least significant bit of the instruction register 7. The second OR gate 9 makes a logical sum of these signals S<sub>0</sub> and S<sub>1</sub>, and outputs it as a signal S<sub>3</sub>.

The microcomputer comprises a pair of selection circuits 10 and 11. The first selection circuit 10 receives at its inputs the signal S<sub>0</sub>, which is the content held in the least significant bit of the bank address register 6 and the logical sum signal S<sub>2</sub>. The first selection circuit 10 receives at its third input a timing signal T, and outputs either one of the signals S<sub>2</sub> and S<sub>3</sub>, as the signal S<sub>4</sub>, in response to the variation of the timing signal T. That is, when the timing signal T is at higher level "1" which means the timing to read out the data in the register B, the first selection circuit 10 selects the logical sum signal S<sub>2</sub> as the output signal S<sub>4</sub>, while, when the timing signal T is at lower level "0" which means the timing to write the data in the register A, the first selection circuit 10 selects the signal S<sub>0</sub> as the output signal S<sub>4</sub>. The second selection circuit 11 also receives the signal S<sub>1</sub>, which is the content b<sub>1</sub> held in the most significant bit of the bank address register 6 and the logical sum signal S<sub>3</sub>. The second selection circuit 11 receives also at its third input the timing signal T. When the timing signal T is "1", the second selection circuit 11 selects and outputs the logical sum signal S<sub>3</sub>, while, when the timing signal T is "0", it selects and outputs the signal S<sub>1</sub>, as its output signal S<sub>5</sub>.

The relation between the timing signal T and the bank designating signals S<sub>0</sub> and S<sub>1</sub> is illustrated in Table 2.

Table 2

	Timing signal	Bank designating signal	Bank designating signal
	T	S <sub>0</sub>	S <sub>1</sub>
Read	1	S <sub>5</sub>	S <sub>6</sub>
Write	0	S <sub>2</sub>	S <sub>3</sub>

With these bank designating signals S<sub>5</sub> and S<sub>6</sub>, the access control means 5 selects one of the register banks 0 to 3. The selected register bank is put accessible through an interface means (not shown) to, for example, an arithmetic logic unit.

The operation of the microcomputer shown in Fig. 1 will be now explained.

(1) The first transfer instruction ordering that the data in the register B<sub>3</sub> of the register bank 0 is to be transferred to the register A<sub>3</sub> of the register bank 0.

For executing this instruction, the bank address register 6 is set to "00", while the instruction register 7 is set to "10011000". The signal S<sub>7</sub>, which is the least significant bit of the instruction register 7 is then "0". Thus, the first and second OR gates 8 and 9 output respectively as the logical sum signals S<sub>5</sub> and S<sub>6</sub>, the signals S<sub>5</sub> and S<sub>6</sub>, which are the contents of the bits 0 and 1 of the bank address register 6. That is, the first and second OR gates 8 and 9 do not modify the address designated by the bank address register 6.

When the timing signal T is "1" which corresponds to the timing of read, the first and second selection circuits 10 and 11 output respectively the logical sum signals S<sub>5</sub> and S<sub>6</sub>, which are now equal to the signals S<sub>5</sub> and S<sub>6</sub>. Thus, the signals S<sub>5</sub> and S<sub>6</sub> are inputted as the bank designating signals S<sub>5</sub> and S<sub>6</sub> to the decoder 5 and then the decoder 5 puts a register bank having address "00" in accessible condition. Accordingly, the register bank 0 is selected and the data contained in the register B<sub>3</sub> is read out.

Next, when the timing signal becomes to the lower level "0", the first and second selection circuits 10 and 11 select respectively the signals S<sub>5</sub> and S<sub>6</sub>, which are the contents of the bits 0 and 1 of the bank address register 6. Accordingly, the access control means or decoder 5 are inputted with the signals S<sub>5</sub> and S<sub>6</sub>, as the bank designating signals S<sub>5</sub> and S<sub>6</sub>, and selects the register bank 0. Thus, the data read out from the register B<sub>3</sub> of the register bank 0 is written in the register A<sub>3</sub> of the register bank 0.

As explained above, the data is transferred from the register B<sub>3</sub> of the register bank 0 to the register A<sub>3</sub> of the register bank 0.

(2) The second transfer instruction ordering that the data stored in the register B<sub>3</sub> of the register bank 3 is to be transferred to the register A<sub>3</sub> of the register bank 0.

In this case, the bank address register 6 is set to "00" and the instruction register 7 is set to "10011001". Then, the signal S<sub>7</sub>, which is the least significant bit of the instruction register 7 is "1". The first and second OR gates 8 and 9 are inputted with "1" at one input thereof to thereby output "1" as the logical sum signals S<sub>5</sub> and S<sub>6</sub>, regardless of the other inputs which are the contents held in the bits 0 and 1 of the bank address register 6.

When the timing signal T is "1", the first and second selection circuits 10 and 11 output respectively the logical sum signals S<sub>5</sub> and S<sub>6</sub>, as the bank designating signals S<sub>5</sub> and S<sub>6</sub>, which are now "1". Thus, with these designating signals S<sub>5</sub> and S<sub>6</sub>, the access control means 5 selects the register bank 3 of which the address is "11". Accordingly, the data stored in the register B<sub>3</sub> of the register bank 3 is read out.

Next, when the timing signal T is "0", the first and second selection circuits 10 and 11 select respectively the signals S<sub>5</sub> and S<sub>6</sub>, which are the contents held in the bits 0 and 1 of the bank address register 6, which are "0" in this case. Thus, the access control means 5 selects the register bank having the address held in the bank address register 6, which is in this case the register bank 0. Accordingly, the data which has been read from the register B<sub>3</sub> of the register bank 3 is written in the register A<sub>3</sub> of the register bank 0.

As readily understood from the above, the data transfer from the register B<sub>3</sub> of the register bank 3 to the register A<sub>3</sub> of the register bank 0 can be executed by only one instruction.

In this example, with the transfer instruction of "10011001", the data stored in the register belonging to the register bank 3 is read and transferred. On the other hand, the register bank to which the data is to be transferred can be designated by setting its address in the bank address register 6. That is, the data can be transferred to the register belonging to any one of the register banks 0 to 3 by setting the address thereof in the bank address register 6.

Although the data transfer has been explained in the above, the add instruction can be executed in the similar manner with the data stored in different register banks.

The code of the first add instruction ordering that the data stored in the registers A and B of the same register bank are added with each other and the result is to be stored in the register A is expressed for example as

"01011000". On the other hand, the code of the second add instruction for executing an addition of the data stored in the same register bank or different register banks is expressed as "01011001".

When the bank address register 6 is set to "00", the first add instruction is executed by, first, reading the data stored in the register B, of the register bank 0, and reading the data stored in the register A, of the register bank 0, adding these data with each other and storing the result in the register A, of the register bank 0. The second add instruction is executed by reading the data stored in the register B, of the register bank 3 and then the data stored in the register A, of the register bank 0, adding these data with each other and storing the result in the register A, of the register bank 0.

As seen from the above, the addition of the data stored in the registers belonging to the register banks 0 and 3 can be executed by one instruction.

Further by changing the polarity of the timing signal T, the direction of the data transfer can be changed. That is, when the polarity of the timing signal T is inverted so that the timing signal T is at lower level "0" when the data in the register B is to be read and the timing signal T is at higher level "1" when the data is to be written in the register A, the transfer of data is conducted in an opposite direction to that in the above explained cases. In more detail, when the bank address register 6 is set to "00", the data is transferred from the register B, of the register bank 0 to the register A, of the register bank 0 in the execution of the first transfer instruction. In the second transfer instruction, the data is transferred from the register B, of the register bank 0 to the register A, of the register bank 3.

Fig. 2 shows another embodiment of the present invention. The microcomputer shown in Fig. 2 is designed for the data processing in a same register bank or between the register banks 0 and 1 or between the register banks 2 and 3. Thus, the computer shown in Fig. 2 has a similar construction as that shown in Fig. 1 except that the signal S<sub>1</sub>, that is, the content held in the most significant the bit of the bank address register 6, is directly inputted to the access control means 5. Namely, the computer shown in Fig. 2 does not include the second OR gate 9 nor the second selection circuit 11 shown in Fig. 1.

In this example, only the content held in the least significant the bit of the bank address register 6 may be modified by means of the OR gate 8. When the timing signal T is "0", the selection circuit 10 outputs the signal S<sub>1</sub>, which is the content held in the least significant bit of the bank address register 6. When the timing signal T is "1", the selection circuit 10 outputs the signal S<sub>1</sub> which has been obtained by modifying the signal S<sub>1</sub> by the OR gate 8.

Thus, the computer shown in Fig. 2 operates as follows:

In the case of the first data transfer instruction which orders data transfer in a same register bank, the instruction code is "10011000". Then, the signal S<sub>1</sub>, which is the least significant bit of the instruction register 7, is "0". The OR gate 8 outputs the signal S<sub>1</sub>, without modifying the same. Thus the bank designating signal S<sub>1</sub> outputted from the selection circuit 10 is equal to the signal S<sub>1</sub>, regardless of the variation of the timing signal T. The access control means 5 always selects the same register bank as that designated by the bank address register 6. Accordingly, with the first data transfer instruction, the data are transferred between the registers belonging to a same register bank.

On the other hand, in the case of the second data transfer instruction, the instruction code is, for example, "10011001". Then, the signal S<sub>1</sub> of "1" is inputted to an input of the OR gate 8 which, in return, outputs the signal S<sub>1</sub> of "1" to the selection circuit 10 by modifying the signal S<sub>1</sub>. Thus, when the bank address register 6 is set to "00" or "10", the OR gate 8 modifies the signal S<sub>1</sub> to "1". Accordingly, at the upper level "1" of the timing signal T, the selection circuit 10 selects the signal S<sub>1</sub>, and thus the access control means 5 designates a register bank having an address of "01" or "11".

At the lower level "0" of the timing signal T, the selection circuit 10 selects the signal S<sub>1</sub> as the bank designating signal S<sub>1</sub>, which is now "0" and then the access control means 5 selects the same register bank as designated by the bank address register 6. That is, when the bank address register is set to "00" or "10", the data transfer is executed between the register banks 0 and 1 or between the register banks 2 and 3. On the other hand, when the bank register 6 is set to "01" or "11", the OR gate 8 outputs the signal S<sub>1</sub> as it is. That is, the data transfer is executed in a same register bank, even with the second data transfer instruction.

Fig. 3 illustrates the third embodiment of the present invention. The microcomputer shown in Fig. 3 has the same construction as that shown in Fig. 2 except that an Exclusive OR gate 12 is employed in lieu of the OR gate 8.

In the case of the first data transfer instruction of which the code is "10011000", the first input S<sub>1</sub> of the Exclusive OR gate 12 is "0" and thus the Exclusive OR gate 12 does not modify the another input signal S<sub>1</sub>. Accordingly, the data transfer is executed in a same register bank.

On the other hand, in the case of the second data transfer instruction of which the code is "10011001", the signal S<sub>1</sub> is "1". Thus the Exclusive OR gate 12 modifies the another input signal S<sub>1</sub>, and outputs it as the signal S<sub>1</sub>. When the bank address register 6 is set to "00", the Exclusive OR gate 12 outputs the signal S<sub>1</sub> of "1". At the upper level "1" of the timing signal T, the selection circuit 10 selects the signal S<sub>1</sub> as the bank designating signal S<sub>1</sub>, and thus, with the inputs of S<sub>1</sub> and S<sub>1</sub>, which are respectively "1" and "0", the access control means 5 designates the register bank 1. At the lower level "0" of the timing signal T, the selection circuit 10 selects the signal S<sub>1</sub>, which is now "0", and the access control means 5 selects the register bank 0. Thus, the data is transferred from a register of the register bank 1 to a register of the register bank 0.

To the contrary, the bank address register 6 is set to "01", the data is transferred from a register of the register bank 0 to a register of the register bank 1 with the second data transfer instruction. That is, in this example, the register banks 0 and 1 constitute a pair of register banks between which data can be transferred.

Further, the same result can be obtained when the bank address register 6 is set to "10" and "11". That is, the register banks 2 and 3 constitute a pair of register banks between which data can be transferred.

As explained above, in the microcomputer according to the present invention, the transfer or processing of the data between different register banks can be executed by only one instruction. Accordingly, the program steps can be largely reduced and the data processing can be executed at a high speed.

Although the present invention has been described in its preferred forms by way of examples, it is understood that changes and variations may be made without departing from the spirit or scope defined by the attached claims.

Although the above examples have been illustrated with a bank register of two bit length and an instruction register of eight bit length, these registers may have other bit length. Further, number of the logical gates and the selection circuits is not restricted to those described in the examples.

#### Claims

1. A microcomputer which includes a plurality of register banks each consisting of a plurality of registers for containing data therein, a bank address register for holding the address of one of said register banks to be accessed and access control means responsive to a bank address signal for putting one of said register banks in accessible condition, said microcomputer comprising:
  - a logic gate circuit receiving at one input at least one bit of the address held in the bank address register and at another input a predetermined portion of the code of an instruction to be executed by the microcomputer and for modifying the inputted bit of the bank address; and
  - a selection circuit for selecting any one of the modified bit and the non-modified bit of the bank address and outputting the selected bit as at least a portion of the bank address signal to said access control means.
2. A microcomputer as claimed in Claim 1, wherein said logic gate circuit is constituted by an OR gate.
3. A microcomputer as claimed in Claim 1, wherein the address of the register bank is expressed in two bits.
4. A microcomputer as claimed in Claim 3, wherein the logic gate circuit comprises a first OR gate receiving at one input the least significant bit of the address held in the bank address register and at another input the least significant bit of the code of an instruction to be executed by the microcomputer and a second OR gate receiving at one input the most significant bit of the address held in the bank address register and at another input the least significant bit of the code of the instruction to be executed by the microcomputer.
5. A microcomputer as claimed in Claim 4, wherein the selection circuit comprises a first selection circuit receiving the output of the first OR gate and the least significant bit of the address held in the bank address register and for selecting any one thereof, and a second selection circuit receiving the output of the second OR gate and the most significant bit of the address held in the bank address register and for selecting any one thereof.
6. A microcomputer as claimed in Claim 5, wherein the first and second selection circuits are responsive to the variation of a timing signal to select one of the inputted signals.
7. A microcomputer as claimed in Claim 1, wherein the instruction code has a length of 8 bits.
8. A microcomputer as claimed in Claim 1, wherein said logic gate circuit is constituted by an Exclusive OR gate.
9. A microcomputer as claimed in Claim 8, wherein the Exclusive OR gate receives at one input the bit 0 of the address held in the bank address register and at another

input the least significant bit of the code of an instruction to be executed by the microcomputer.

10. A microcomputer as claimed in Claim 9, wherein the address of the register bank is expressed in two bits.
11. A microcomputer as claimed in Claim 9, wherein the selection circuit is responsive to the variation of a timing signal to select one of the two inputted signals.
12. A microcomputer as claimed in Claim 9, wherein the instruction code has a length of 8 bits.
13. A microcomputer which includes a plurality of register banks each consisting of a plurality of registers for containing data therein, a bank address register for generating the address of one of said register banks to be accessed and access control means responsive to a bank address signal for putting one of said register banks in accessible condition, said access control means comprising:
  - first means for receiving the address of said address register;
  - second means for receiving information indicating a different register bank to be selected;
  - third means responsive to said address and said information for generating an actually selecting signal; and
  - fourth means for applying said actually selecting signal to one of said register banks.

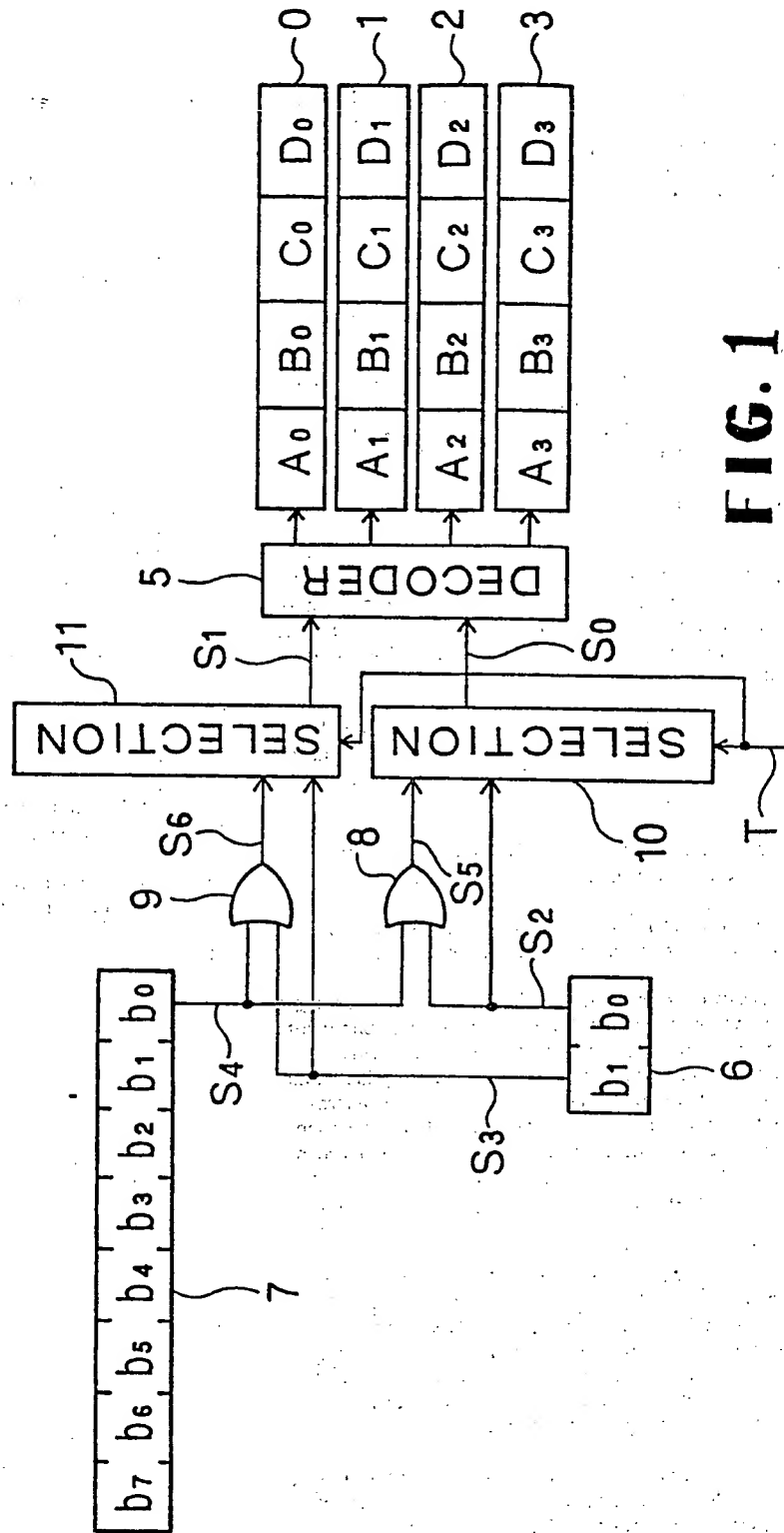
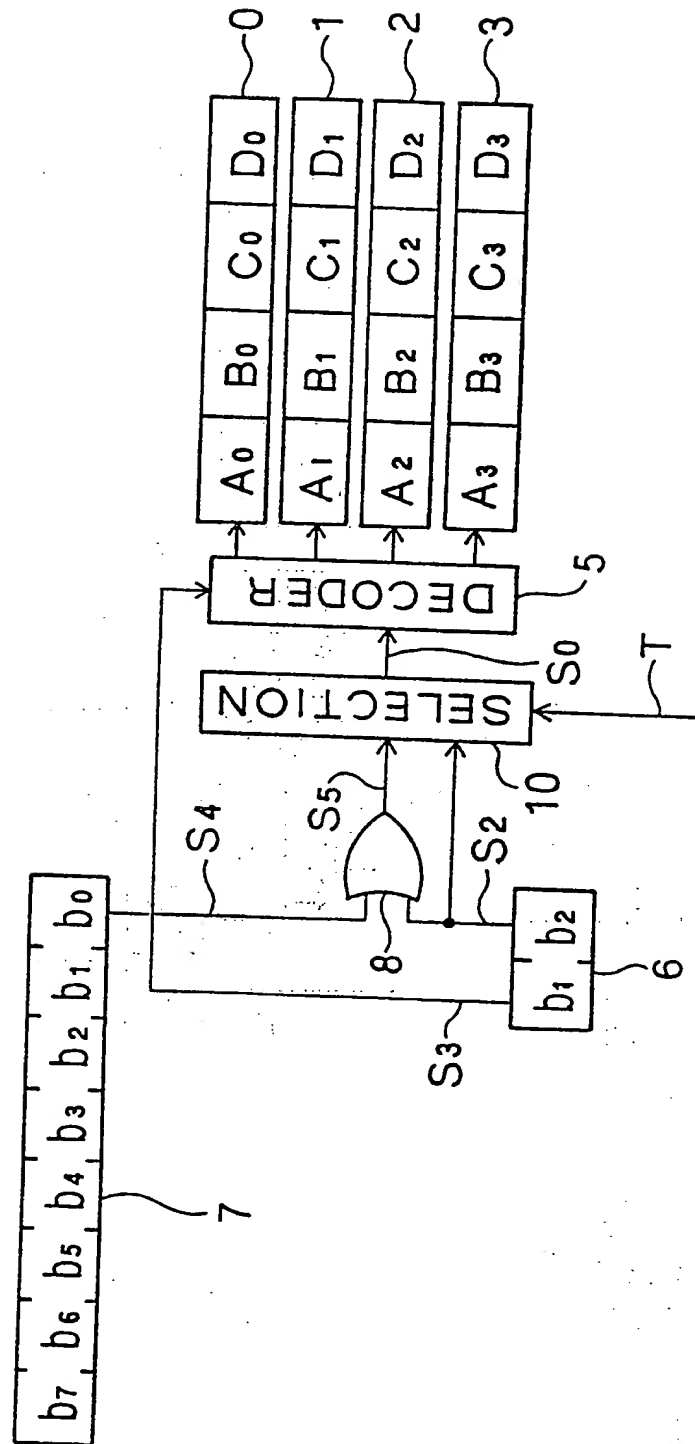


FIG. 1



**FIG. 2**



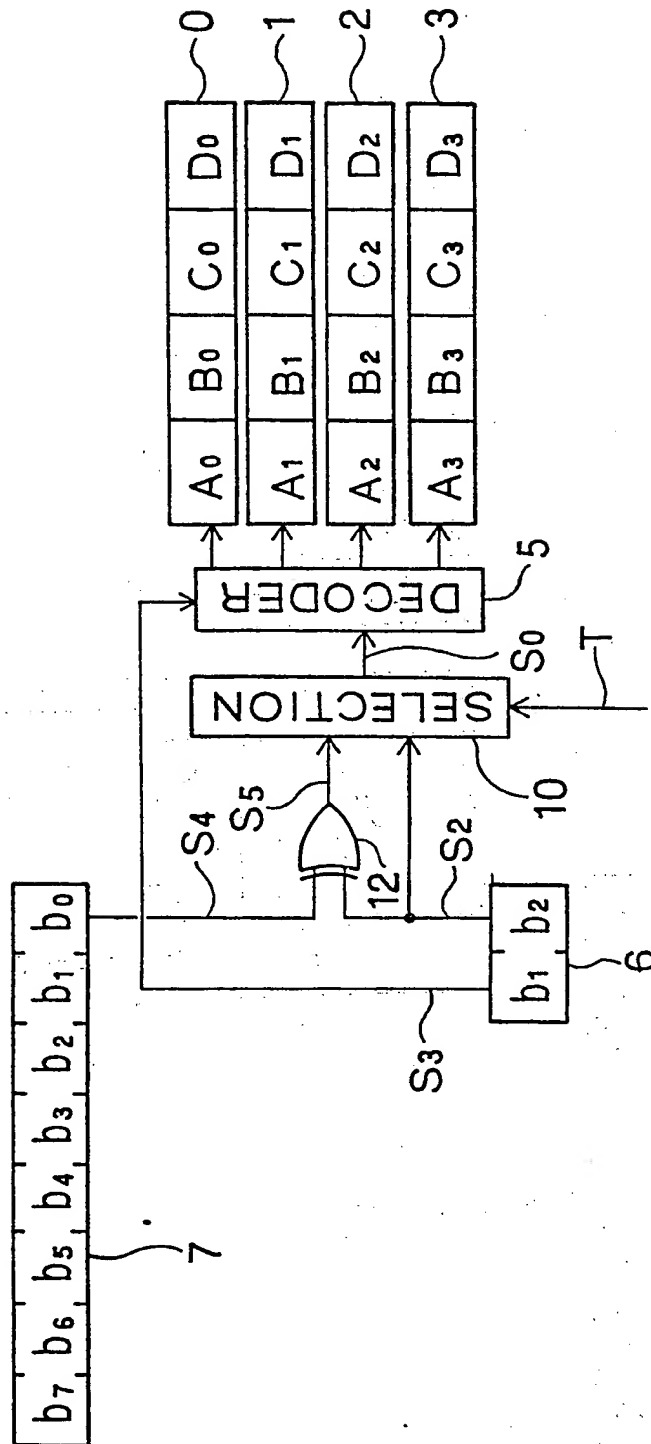


FIG. 3

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